AF-2811 $

#1 Not. of Appeal YR 10/28/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of LEROUX

Atty. Docket US008082

Serial No. 09/737,606

Group Art Unit 2811

Filed: 12/14/2000

Examiner Magee, T.

Title: A SELF-COMPENSATING MARK DESIGN FOR STEPPER ALIGNMENT

Mailstop APPEAL
Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NOTICE OF APPEAL

Sir:

Applicant(s) hereby appeal(s) to the Board of Patent Appeals and Interferences from the decision dated 2/27/2003 of the Examiner finally rejecting claims 1, 2 and 4-7.

[X] Please charge the fee of $320.00 to Deposit Account No. 14-1270.

[*] No additional fee is required, because the fee was paid in a prior appeal.

Respectfully submitted,

By _____
Michael J. Ure
Attorney
(408) 474-9077

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited this date with the United States Postal Service as first-class mail in an envelope addressed to: ASSISTANT COMMISSIONER FOR PATENTS, Alexandria, VA 22313-1450

On 8/13/2003
(Date of Mailing)

By _____
(Signature)

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I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE WITH SUFFICIENT POSTAGE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C., 20231, ON:

Date: 8/13/2003 By: [signature]

#15. Appeal Brief 10/28/03

PATENT
Attorney's Docket No. US008082

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
LEROUX	Group Art Unit: 2811
Application No.: 09/737,606	Examiner: Magee, T.
Filed: 12/14/2000	**Appeal No.**_____
For: A SELF-COMPENSATING MARK DESIGN FOR STEPPER ALIGNMENT	

BRIEF FOR APPELLANT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

This appeal is from the decision of the Primary Examiner dated 2/27/2003, finally rejecting claims 1, 2 and 4-7, which are reproduced as an Appendix to this brief.

The Commissioner is authorized to charge the fee of $160, and any other fees that may be required by this paper, to Deposit Account No. 14-1270.

(1) Real Party in Interest

The real party in interest is the assignee, Philips Electronics North American Corporation.

(2) Related Appeals or Interferences

Applicant is not aware of any related appeals or interferences.

(3) Status of Claims

Claims 1-14 remain pending in the present application. Claim 3 has been indicated as containing allowable subject matter. All other claims have been finally rejected and are on appeal.

(4) Status of Amendments

All amendments have been entered. No amendment after final has been submitted.

(5) Summary of the Invention

The present invention relates to the arrangement of alignment targets on semiconductor wafers and the use of such alignment targets in the operation of a stepper scanner. A stepper scanner exposes different areas of a semiconductor wafer in sequence through a mask or reticle to selectively expose (pattern) a photoresist layer. A set of masks (e.g., from about 5 to about 20) is required to fabricate a finished semiconductor wafer. Precise alignment of the patterns formed using different masks of the mask set is required. Alignment targets are pro-

vided for this purpose. Alignment targets are formed within a scribe-line area between individual integrated circuits at the boundaries of a stepper shot. (The number of integrated circuits imaged within a stepper shot depends on the size of the integrated circuit.) During stepping, the wafer is moved on a stage relative to the stepper scanner. In order to arrive at the final relative position of the wafer and the mask held by the stepper scanner, fine alignment is performed based on the alignment targets.

In the present invention, as recited in claim 1-3, for example, alignment targets are arranged in one or more mirror-image pairs. This arrangement allows *translational error* and *rotational error* to be distinguished. In one exemplary embodiment, alignment targets are located at the midpoint of each side of the stepper shot. In another exemplary embodiment, alignment targets are located at each of the corners of the stepper shot. In the acknowledged prior art (Figure 2A of the present specification), by contrast, one alignment target is located in the X-axis direction along a boundary of the stepper shot, and another alignment target is located in the Y-axis direction along a boundary of the stepper shot.

(6) The References

The rejection is based principally on Zhou, U.S. Patent 6,172,409.

Zhou relates to a particular arrangement of an alignment target that is advantageous where CMP (chemical mechanical polishing) of a wafer bearing such alignment targets occurs between successive exposure steps. CMP is used to planarize the wafer surface, thereby preparing the wafer for the subsequent exposure step.

The alignment target of Zhou features a principal inner alignment pattern and a surrounding outer "buffer structure." As noted in the Abstract, "The buffer structure thus helps to preserve the alignment marks...."

Also applied against the claims are: 1) promotional literature describing the Ultratech stepper; 2) the well-known semiconductor processing text by Wolf and Tauber; and 3) a technical paper by Banks.

The teachings of these latter references are not believed to bear on the patentability of the principal claims.

(7) The Rejection

In the Final Rejection of 2/27/2002, claims 1, 2 and 4-7 were rejected as being unpatentable over Zhou in view of Ultratech. The rejection states in part:

> [I]t is well known that the shot can be made to overlap several die with the scribe lines at an edge of the shot perimeter (See Ultratech ....) Further, the shot size can be adjusted to include several die with alignment marks at first and second sides, where the alignment targets are at midpoints of a side of stepper shot.

> The rejection also states (Final Rejection, paragraph number 8):

> In addition, Zhou discloses alignment targets at midpoints and in "mirror" images for alignment.

Claims 4 and 5 were rejected as being unpatentable over Zhou in view of Ultratech, further in view of Wolf and Tauber. The rejection states in part:

> Hence, it would have been obvious ... to add Wolf et al. and Banks to Zhou to obtain a process for producing alignment targets by a positive or negative photoresist step onto scribe lines of a wafer surface to form raised or

depressed target features.

(8) Issues

The only issue presented is whether claims 1, 2 and 6 would have been obvious based on Zhou in view of Ultratech. For purposes of the present appeal only, claim 4, 5 and 7 are considered to stand or fall with independent claim 1.

(9) Argument

The alignment target of Zhou features a principal inner alignment pattern and a surrounding outer "buffer structure." As noted in the Abstract, "The buffer structure thus helps to preserve the alignment marks...."

Zhou, however, simply teaches the arrangement of a single alignment target. Zhou does not address the number or relative positions of alignment targets within a stepper shot. It is in these details that the advantages of the present invention are obtained.

In particular, as recited in claim 1-3, alignment targets are arranged in one or more mirror-image pairs. This arrangement allows translational error and rotational error to be distinguished. In one exemplary embodiment, alignment targets are located at the midpoint of each side of the stepper shot. In another exemplary embodiment, alignment targets are located at each of the corners of the stepper shot.

Zhou says nothing about this feature of the invention. Similarly, Ultratech says nothing about this feature of the invention.

The contention that "Zhou discloses alignment targets at midpoints and in 'mirror' images for alignment" is incorrect. An alignment *target* comprises multiple alignment *marks*. In the cover figure of Zhou, what is illustrated is a single alignment target comprising multiple alignment marks. In Zhou, the alignment target exhibits bilateral symmetry. That is, relative to the center of the alignment target, corresponding alignment marks may be identified on either side of the center, having midpoints corresponding to the center. The present invention does not concern the arrangement of an individual alignment target.

Rather, the invention concerns the arrangement of multiple alignment targets relative to a stepper shot as is clear from a reading of claim 1. Zhou simply is not concerned with the arrangement of multiple alignment targets relative to a stepper shot.

Ultratech makes mention of alignment targets at line 4 of the **Description.** The mere mention of alignment marks does not teach or suggest the particular features of claim 1.

(10) CONCLUSION

For the foregoing reasons, claims 1, 2 and 6 would not have been obvious based on Zhou in view of Ultratech.

Applicant respectfully submits therefore that the Final Rejection should be REVERSED.

Respectfully submitted,

By: _____
Michael J. Ure
Attorney for Applicant
Registration No. 33,089

Date: August 13, 2003

APPENDIX OF CLAIMS

1. A wafer for fabricating integrated circuits using a stepper, said wafer comprising:

a first region for receiving a four-sided stepper shot, said stepper shot having a scribe line along its perimeter; and

four alignment targets disposed within said scribe line, said alignment targets for aligning said step shot and said first region;

wherein one alignment target is located on each side of said stepper shot, and wherein an alignment target on one side of said stepper shot and an alignment target on a second side of said stepper shot opposing said first side are located in mirror-image positions.

2. The wafer as recited in claim 1 wherein opposing sides of said stepper shot are equal in length, and wherein an alignment target is located at each mid-point of a side of said stepper shot.

4. The wafer as recited in claim 1 wherein said alignment targets are formed according to a positive resist process.

5. The wafer as recited in claim 1 wherein said alignment targets are formed according to a negative resist process.

6. The wafer as recited in claim 1 further comprising a second region adjoining said first region, said second region for receiving a second stepper shot having a scribe line along its perimeter, wherein a segment of said scribe line of said second stepper shot overlays a segment of said scribe line of said first stepper shot such that an alignment target of said second stepper shot overlays an alignment target of said first stepper shot.

7. The wafer as recited in claim 1 wherein each of said alignment targets comprises a plurality of rectangles.